a trench in the substrate;

an oxide liner formed lining the trench and a top surface of the substrate;

a nitride liner recessed within said trench and the nitride liner forming a partially enclosed volume, said partially enclosed volume being completely filled with a dielectric material which also completely fills the trench;

an uppermost surface of said nitride liner being disposed just below a transistor channel depth, Dc, of a transistor disposed in a well beside said shallow trench isolation structure, the recessed nitride liner being dimensioned and configured to prevent hot carrier effects due to charge trapping for charge which traverses a channel of the transistor;

an oxide fill disposed above said nitride liner, such that said oxide fill extends above and below the uppermost surface of said nitride liner substantially to a top surface of said substrate and completely filling below the uppermost surface, respectively; and

the oxide fill is disposed above said nitride liner such that polysilicon material used in other processing is prevented from entering the trench.

REMARKS

This application has been reviewed in light of the Office action dated April 5, 2000. Claims 1-5, 7 and 24 and 25 are pending in the application. Claim 24 has been amended. No new matter has been added by the amendment. The Examiner's reconsideration of the rejection in view of the amendments and the following remarks is respectfully requested.

By the office action, claims 1 and 24 stand rejected under 35 U.S.C. 112 first paragraph, as containing subject matter which was not described in the original specification, in such a way to reasonably convey to one skilled in the relevant art that the inventors had possession of the claimed invention at the time the application was filed. The Applicant respectfully disagrees.

"An uppermost surface of said nitride liner being disposed just below a transistor channel depth," as set forth in claims 1 and 24 is described, for example, in the present specification at page 9, lines 21 to 26, and shown in FIGs. 6 and 8. The specification clearly states that the nitride liner is below the channel depth of a transistor. The claim language " just below" is a subset of this feature and is therefore not only sufficiently disclosed, but narrower in scope than the